Printed Electronics Workflow

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ABSTRACT

As corporations and universities continue to research and develop inkjet printing, it is increasingly becoming a more viable electronics manufacturing technique. With the relatively low setup costs, greater design freedom with the use of many different substrates and printable materials, and significantly faster prototyping, printed electronics is gaining traction in academic, commercial, and even do-it-yourself communities. Unfortunately, this technology still lacks a standardized design flow. There are several competing printer manufacturers selling design kits and materials that are meant to only be used with their hardware. This makes collaboration and experimental replication difficult. It was our goal to develop a configurable design flow for the design, simulation, verification, and printing of printed electronics that is meant to work with all printing materials and printers. We have created several tutorials that guide users through the process of configuring their process design kit (PDK), and we look to automate this process in the future. We have added an N-type layer, a new N-type organic thin-film transistor (OTFT) device with PCell, a SPICE model for the device, and LVS and DRC rules to the existing Organic PDK (OPDK). Finally, we simulated an inverter using our new parameterized N-type OTFT. Our future work will include completing and automating the workflow, extending the models, and finally printing devices.

1. INTRODUCTION

Printed electronics has recently gained traction as a viable electronics design technology. When compared to the traditional photolithographic process currently being used for mass MOSFET IC production, it has several significant advantages including very low setup costs, fast prototyping, and the capability of printing electronics on flexible substrates. Printable electronics really has opened up the design of integrated circuits to a whole new set of design freedoms and research potential. Not only does the designer have a large array of organic materials that they can choose to print with, but they can choose to print on flexible substrates, and all on a printer that fits on a kitchen table.

Unlike photolithographic processes, printing electronics is still largely a manual process with a workflow that is composed of several disjoint tools. Several factors lead to large variations that make the integration and automation of this process difficult. First, there are many different material printers available that can be used for printing organic inks. Each printer has different tolerances, minimum and maximum feature sizes, different numbers of nozzles, and other characteristics. Second, most inks are created by dissolving powder in a solvent such as water, tetradecane, or triethylene. This manual process results in ink properties that are not consistent across mixings to the degree required for the precise prediction of properties or replication. This set of variations motivates our research in designing a generic, configurable workflow that will work across a set of printers and inks.

Every electronics printer user must design their circuits by manually updating their PDK to include the layers that they wish to print, and the characteristics of their printer. DRC and LVS files are also manually updated to the ink and printer types being used. Finally, many materials printer manufacturers provide software support for their devices which does not work on other manufacturers' printers; it is often proprietary and not available for download. This non-standard and disjoint set of tools stifles the potential to collaborate and makes reproducing research results remarkably difficult.

It is our intent to create an open source design flow for printed electronics that extends from design to printing. The TDK4PE Technology & Design Kit for Printed Electronics Group is a European coalition looking to accomplish the same goal, but they are still working on the Design Kit and plan to be done in September 2014. It is our hope to cooperate with them and create an open source design workflow solution [1]. It is our goal to create tutorials to allow researchers the ability to update their tools and begin printing. Future work will look into automating this process as much as possible to create one end-to-end process.

2. OVERVIEW

In order to achieve this goal of a configurable design flow, we will start by creating a set of tutorials that will serve as a guide for printer users to configure their workflow to the printer and inks that they are using. The major components that must be configured are the Layer Definitions, Design Rule Check (DRC), Layout vs. Schematic (LVS), Pcell definitions and model files. These configurations are defined in the PDK.

3. PROCESS DESIGN KIT (PDK)

The Process Design Kit (PDK) contains layer definitions, Design Rule Check rule sets, Layout Vs. Schematic rule sets, Pcell definitions and models for simulation. The University of Minnesota created an Organic PDK (OPKD) that was developed for printing Organic Thin Film Transistors (OTFT) [2]. The OPDK supports two types of transistors, a PFET with a P3HT Channel (PTFT_P3HT_TG) and a FET with a CNT channel, TFT_CNT_TG, which is effectively a pass-gate transistor. One shortcoming of the layers offered in the OPDK is that there is no available N-type OTFT. In order to extend the OPDK and allow for more design alternatives, we wanted to add an N-type layer to the OPDK and add an N-type TFT device. We chose to add Poly(benzimidazobenzophenanthroline), or BBL for short, because it was one of few N-type semiconducting organic materials being offered by ink manufacturers [3].

We added the BBL layer into the TechFile and created a tutorial for adding new layers, which can be found at:

https://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassEE6332Fall12Group-Tutorial-Adding_a_New_Layer.

4. LAYOUT

In addition to adding a new layer, we also created NTFT_BBL_TG, an N-type OTFT and the parameterized cell (PCell) for it. This device functions in the same way that an NMOS does; we chose to use the same model as an NMOS device for simulation. We chose to add a Pcell for this device because it makes layout designs easier for the developer. Instead of drawing each polygon for the NTFT_BBL_TG, all the designer needs to do is open the PCell, set the Width and Length parameters, and drop it onto their substrate. We then created tutorials for adding a new Device and Pcell, which can be found at:

https://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassEE6332Fall12Group-Tutorial-Adding_a_New_Device

https://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassEE6332Fall12Group-Tutorial-Adding_a_New_PCell

5. MODEL

Another important component in the OPDK is the model defining the devices. A model is an hSpice representation of the electrical characteristics of a device defined in the PDK. We chose to add a model for the NTFT_BBL_TG device so that we could simulate the device. Instead of extracting the parameters from a printed device, we took the model definition of the N-type component of the TFT_CNT_TG device. The OPDK models TFT_CNT_TG, effectively a pass gate, as an N-type and a P-type transistor connected in parallel. We copied the N-type characteristics and used this information for our model. Figure 3 shows the Voltage Transfer Curve (VTC) of our inverter that we constructed from the OPDK P-type transistor and our custom BBL N-type transistor. Although this diagram shows a high V_M, the inverter did invert. Figures 1, 2, and 3 show the schematic of our inverter, the layout of the N-type OTFT, and the VTC of our inverter, respectively.

We expect that after printing our first transistors, we will update the models and get a more realistic model for our devices. We also created a tutorial on adding models to devices, which can be found at:

https://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassEE6332Fall12Group-Tutorial-Adding_a_New_Model

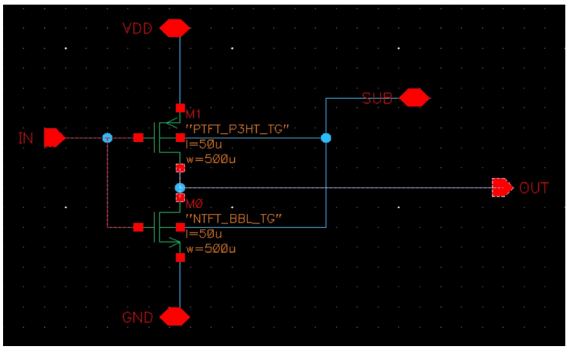

Figure 1—Schematic of an inverter using OTFTs. It mimics the design of a CMOS inverter by using complementary N- and P-type transistors, made from BBL and P3HT, respectively. The SUB pin is required by the model and is connected to GND.

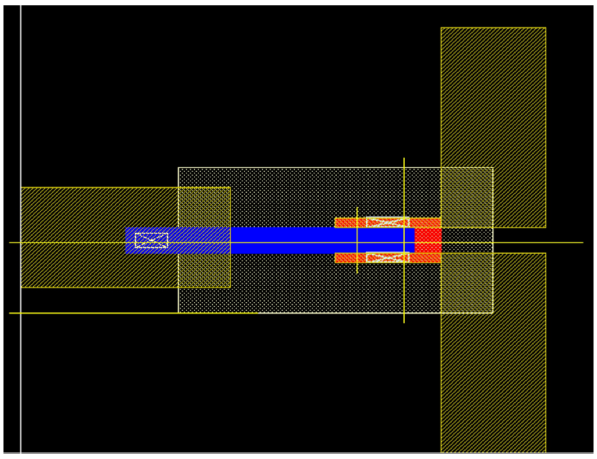

Figure 2—Layout of a P-type OTFT. The red section is P3HT, which is used as the semiconductor.

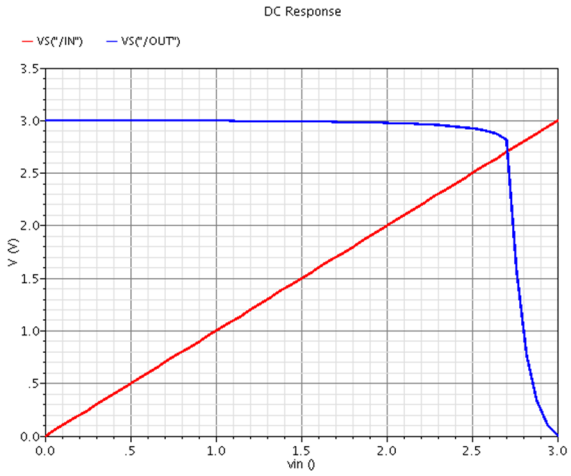

Figure 3—Voltage transfer curve for our organic inverter. The main concern with it is that $V_M = 2.71\,\mathrm{V}$, well above $V_{DD}/2$. We chose not to change our model because we expect to refine it after parameter extraction.

6. DESIGN RULE CHECK (DRC)

The design rule check stage checks the layout to ensure that it adheres to rules created by the intended fabricator so that the design is realizable. These rules include minimum width of a layer, minimum spacing between edges of a layer, minimum spacing between edges of two different layers, and which layers are allowed to overlap and how. Some layers may never overlap, while others must completely overlap. For silicon-based processes, these rules are provided by the fabrication facility that the designer intends to use to realize his design. For printed electronics, design rules are dependent upon the printer, printed materials, and substrate. Electronics printer users will need to be able to easily change design rules to fit their printers.

In Cadence, design rules are defined in `calibreDRC.rul`, in `<PDK_root>/techfile/cadence`. Figure 4 is an example of how these rules are defined.

A Calibre design rule consists of the names of the layers it affects, a comment indicating what the rule is for, and the rules

themselves. Rules indicate overlap of layers (or sets of layers) and how much they must overlap by or be separated by [4].

To facilitate searching and editing this file, we developed a Perl script that opens the rules file and stores its data into a database. The user of the script can then freely search through the different components of the loaded file and add new rules or remove old ones. An in-depth tutorial on how to use this script, along with the script itself, can be found here:

https://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassEE6332Fall12Group-Tutorial-Editing_Design_Rules.

Using this script, we added rules for the BBL layer that are identical to the existing P3HT layer.

```
P3HT_TFT.METAL1.1 {
@P3HT and METAL1 must overlap by 10 um
INTERNAL P3HT and METAL1 < 1
}
```

Figure 4—Example Cadence design rule for minimum spacing between layers. Blue text indicates layers affected by the rule, green text indicates a comment detailing the rule, and red text indicates the syntax of the rule.

7. LAYOUT VS. SCHEMATIC (LVS)

The layout vs. schematic stage checks the layout to make sure it is consistent with the schematic. The designer provides rules to the LVS tool defining how connections and devices are made using material layers. These rules define which layers are present in each device and how they must overlap to form connections within and between them. For example, in an OTFT, the gate is defined as the intersection between the semiconductor, dielectric, and gate terminal layers, but not metal. Overlaps between layers can also be defined as valid connections between devices or wires.

In Cadence, this is defined in `calibreLVS.rul`, which is located in `<PDK_root>/techfile/cadence`. It does not assume anything about any layers in the techfile or nets in the design; as such, power and ground net names must be provided to it. Using `REDUCE` commands, the LVS tool can be instructed to reduce parallel or series devices that have the appropriate connections into a single device. For example, a pair of transistors whose gates, drains, sources, and bulks are all connected to the same respective nets can be simplified into one device. The tool can also be instructed to filter out unused devices. Finally, it must be told what properties of devices must be included in the check, such as width and length for transistors, using the `TRACE PROPERTY` command [4]. A tutorial on how to edit this file, including some important command definitions, can be found here:

https://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassEE6332Fall12Group-Tutorial-Editing_Layout_Versus_Schematic_(LVS)_Rules.

We added LVS rules for a BBL N-type TFT that are the same as those for the existing P3HT TFT.

8. LAYOUT TO BITMAP

Unlike the photolithographic process, the designer is not done when the GDSII file is generated from the layout design by Cadence. The final step before printing is to generate a set of bitmap files that the printer can interpret and use to print. There are several printing companies that sell the tools necessary for this conversion, but we haven't found any available open-source versions. Francesc Vila Garcia, Jofre Pallares Cuxart, and Lluis Teres Teres published a paper in 2010 on a tool that they developed to solve this problem. It is our hope to use Francesc Garcia's Layout2Bitmap program once it has been released.

The Layout to Bitmap tool is a program that reads in a GDSII standard layout format, and using geometric algorithms determines how the shapes can be generated with ink drops [5]. The CMOS process uses masks to project light in shapes on the silicon. Printable electronics are different in that ink drops are the smallest quantum of measurement, and thus all shapes must be composed of overlapping drops.

9. PRINT

This part of the design flow must be configured for the printing technology available. In our case it will be configured for a Dimatix DMP2831 Materials Printer, which uses inkjet printing to transfer material from a cartridge to a substrate. Each droplet is 10 µm in diameter and the printing platen is able to support a substrate about the size of a standard letter size sheet of paper (8.5" x 11") and several centimeters thick. While it cannot be used to print bitmapped images directly, Dimatix Drop Manager, the software used to control it, can convert them into the appropriate format.

10. RELATED WORK

Printed electronics has been an area of intense research for the past several years, but only recently have organizations started to emphasize the importance of a general design workflow. The three major projects hoping to develop this general workflow that we investigated were The University of Minnesota's Organic PDK (OPDK), Francesc Vila Garcia's Layout to Bitmap research, and TDK4PE, a European, cooperative research project with the goal of creating a ubiquitous design methodology for mass printed electronics manufacturing.

The University of Minnesota's OPDK is a Cadence PDK designed for OTFTs with the top-gate design that is based on NCSU's FreePDK open-source PDK. We extended OPDK to include an additional N-type layer, N-type OTFT, design rules, and model called the NTFT_BBL_TG. Our tutorials were also based around extending the OPDK for future additions.

Francesc Garcia's project hoped to accomplish the same goals as we did, but with an emphasis on the Layout to Bitmap tool. He designed this tool, and we hope to incorporate it into our design flow after the tool is released.

We are also in contact with TDK4PE and hope to collaborate with them in the future to develop their design flow. They are also looking to use Garcia's tool as well as the University of Minnesota's OPDK in their design flow.

11. FUTURE WORK

There are several components that we were unable to complete in our design flow. The most significant component is the Layout to Bitmap tool. We have contacted the developer of such a tool, and we are working on getting the source to the program in the next few weeks to months.

Another important component that needs to be done is the addition of layers. For the purpose of this project, we have added one N-type layer to test the N-type TFT device for functionality.

Other layers that need to be added include additional metal materials and potentially other semiconductors for future TFTs.

It is critical that we enhance our models by extracting parameters. This is done by printing transistors that we design in Cadence, and extracting parameters from them. Using this information, we can update the characteristics defined in the model files and be able to print OTFTs with known characteristics.

The most important work in the future lies in creating tools and adding functionality to the OPDK that will allow it to be reconfigurable for different printers, devices, materials, and inks. For example, a major consideration in design rules is the resolution of the printer, which for an inkjet printer is defined at least in part by the droplet size. It should be easy to reconfigure design rules to fit the characteristics of a new printing device. Once an ink has been mixed, it should not be thrown away because it does not fit the parameters of an existing model in the PDK for a material that has the same function; rather, a tool should be created that simplifies adding this new material to the PDK or editing an existing one. New layers, new models, and new devices should be created with little effort. LVS rules should be updated with any new layers created with this tool. A user of this system should never have to learn the syntax of a DRC or LVS rule file or how a new layer or PCell is created.

Once the layout-to-bitmap step is completed, a tool for converting from the bitmapped images to the DMP2831's pattern format automatically without having to go through the Dimatix Drop Manager first will be created. This tool will be updated with new printing devices as they are added if necessary.

12. CONCLUSION

In conclusion, we have begun the steps necessary to create a process design flow for printed electronics. Our current work includes adding a new N-type TFT to the existing OPDK and developing a tool to easily search through and edit design rules. In adding a new device, we have created a new material layer in Cadence, created an N-type TFT PCell with variable length and width, added a SPICE model for an N-type OTFT, and added rules for DRC and LVS. Finally, we created a simple circuit (an inverter) using our new device and verified that the model functions as expected. In the future, work must be done to simplify the process of adding new materials and information to this PDK. New tools must be developed to automate the additions that must be made in order to take differences in printing machinery and ink mixture into account.

13. REFERENCES

[1] TDK4PE Technology & Design Kit for Printed Electronics. http://www.tdk4pe.eu/. December 2012

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